

Appln No. 10/603,362
Amdt date July 14, 2004
Notice of Allowance Dated: June 2, 2004.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-8. (Cancelled)

9. (Currently Amended) A signal processing system comprising:

an interpolator, having one or more interpolation stages, for interpolating an input data signal at a first variable frequency to generate an interpolated output signal at fixed output frequency, wherein at least one of the one or more interpolation stages interpolates by a value of M/N , where N is an integer and M is an integer or a non-integer; and

a frequency control loop coupled to the at least one of the one or more interpolation stages that interpolates by a value of M/N ,

wherein the frequency control loop generates a phase offset signal proportional to M/N as a function of an offset in phase between a variable frequency clock signal at a second variable frequency and a sample clock signal at a sample clock frequency

10. (Previously Presented) The signal processing system of claim 9 wherein the phase offset signal is greater than or equal to zero and less than one.

11. (Previously Presented) The signal processing system of claim 9 wherein the interpolator interpolates the input data signal by a non-integer value.

12. (Previously Presented) The signal processing system of claim 9 wherein the interpolator interpolates the input data signal by an integer value.

Appln No. 10/603,362
Amdt date July 14, 2004
Notice of Allowance Dated: June 2, 2004.

13. (Previously Presented) The signal processing system of claim 9 further comprising a modulator for modulating the interpolated output signal onto a trigonometric signal at a carrier frequency.

14. (Previously Presented) The signal processing system of claim 13 further comprising a digital to analog converter for converting the modulated signal to an analog signal.

15. (Previously Presented) The signal processing system of claim 9 wherein the frequency control loop comprises:

a phase detector that provides an error signal representing phase difference between said variable frequency clock signal at the second variable frequency and a first clock,

a loop filter coupled to said phase detector that filters said error signal,

a numerically controlled oscillator, responsive to said filtered error signal and the sample clock for providing said first clock and said phase offset signal; and

a buffer for receiving an input signal at the variable frequency and responsive to said first clock, outputting a data signal at said first clock frequency.

16. (Previously Presented) A signal processing system comprising:

a frequency control loop for providing a first clock at a first clock frequency as a function of a sample clock having a sample clock frequency and a variable frequency input clock;

a buffer for receiving an input signal at the variable frequency input clock and, responsive to said first clock, outputting a buffered signal comprising a plurality of data bits at said first clock frequency;

a symbol mapper for converting the plurality of data bits in the buffered signal to first and second data signals at said first clock frequency, wherein amplitude and phase of the first and second data signals vary to represent the binary data bits of the buffered signal; and

Appln No. 10/603,362
Amdt date July 14, 2004
Notice of Allowance Dated: June 2, 2004.

a first interpolator coupled to the first data signal and a second interpolator coupled to the second data signal, wherein the first and second interpolators are responsive to the first clock signal for providing first and second interpolated signals at the sample clock frequency.

17. (Currently Amended) A signal processing system comprising:

means for interpolating an input data signal at a first variable frequency to generate an interpolated output signal at fixed output frequency, wherein one or more interpolation stages of the means for interpolating interpolates by a value of M/N , where N is an integer and M is an integer or a non-integer; and

means coupled to the at least one of the one or more interpolation stages that interpolates by a value of M/N , for generating a phase offset signal proportional to M/N as a function of an offset in phase between a variable frequency clock signal at a second variable frequency and a sample clock signal at a sample clock frequency

18. (Previously Presented) The signal processing system of claim 17 wherein the phase offset signal is greater than or equal to zero and less than one.

19. (Previously Presented) The signal processing system of claim 17 wherein the means for interpolating interpolates the input data signal by a non-integer value.

20. (Previously Presented) The signal processing system of claim 17 wherein the means for interpolating interpolates the input data signal by an integer value.

21. (Previously Presented) The signal processing system of claim 17 further comprising means for modulating the interpolated output signal onto a trigonometric signal at a carrier frequency.

Appln No. 10/603,362
Amdt date July 14, 2004
Notice of Allowance Dated: June 2, 2004.

22. (Previously Presented) The signal processing system of claim 21 further comprising means for converting the modulated signal to an analog signal.

23. (Previously Presented) The signal processing system of claim 17 wherein the means for generating a phase offset signal comprises:

means for generating an error signal representing phase difference between said variable frequency clock signal at the second variable frequency and a first clock,

means for filtering said error signal,

means for providing said first clock and said phase offset signal, responsive to said filtered error signal and the sample clock; and

means for receiving an input signal at the variable frequency and responsive to said first clock, outputting a data signal at said first clock frequency.